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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L 21/768 — A1

(11) International Publication Number: WO 00/59031

(43) International Publication Date: 5 October 2000 (05.10.00)

(21) International Application Number: PCT/US00/07652

(22) International Filing Date: 23 March 2000 (23.03.00)

(30) Priority Data:
09/280,767 29 March 1999 (29.03.99) US

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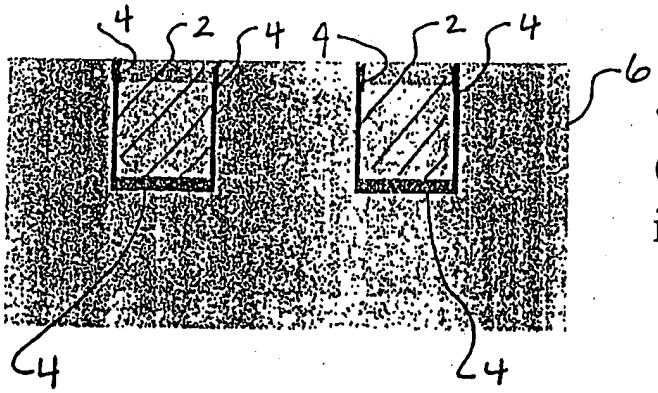
(81) Designated States: DE, GB, JP, KR, SG.

Published
With international search report.

(54) Title: TWO–STEP CHEMICAL–MECHANICAL PLANARIZATION FOR DAMASCENE STRUCTURES ON SEMICONDUCTOR WAFERS



•Oxide polish rate > Cu rate 'repairs' initial topography

(57) Abstract

A method of improving planarity of semiconductor wafer surfaces containing damascene and dual–damascene circuitry using chemical–mechanical polishing techniques. The method includes using a first polishing step to substantially remove excess surface metal (2) up to a detected end point. After rinsing, a second step of chemical–mechanical polishing is applied, using a second slurry that has a higher selectivity for dielectric (16) than metal (2), preferably from 1.8 to 4 or more times greater. The second step of polishing, in accordance with the invention, has been found to substantially eliminate dishing and improve planarity.

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TWO-STEP CHEMICAL-MECHANICAL PLANARIZATION FOR DAMASCENE STRUCTURES ON SEMICONDUCTOR WAFERS

Field of Invention

This invention relates to the fabrication of semiconductors. More particularly, it relates to a chemical-mechanical semiconductor wafer polishing process, for use with wafers that include damascene and/or dual-damascene circuit structures, that substantially reduces "dishing" and erosion to provide improved planarity.

Background of Invention

The fabrication of very large scale integrated circuits on silicon wafers is a process requiring extreme precision because of the very fine details of the circuits. Indeed, the width of circuit lines are continually decreasing, as the technology advances, and are now in the 0.18-100 micron range. Since these circuits are produced using photolithographic techniques, extremely accurately ground lenses are required to provide such fine detail. As a necessary consequence of providing such precise focusing, the lenses lack depth of field, i.e. an image is accurately produced only at a specific distance from the lens, and any deviation in this distance produces an increasingly unfocused or fuzzy image. Therefore, the surface onto which the image is projected must be as perfectly planar as possible to eliminate out of focus image fuzziness. A failure to maintain planarity exacerbates the problem as additional layers are formed on the surface resulting in an increased proportion of defective semiconductors that must be rejected.

A standard technique for restoring surface planarity after inlaying metal in dual-damascene structures within a dielectric layer, is chemical-mechanical planarization (CMP). During this process, the surface of the wafer is polished at select intervals, with a polishing pad and a chemical slurry, to remove excess metal and to replanarize it. The slurries contain an abrasive such as silica or alumina, and chemical additives that are designed to selectively react with and soften the composition of those components that must be planarized on the wafer surface. Accordingly, polishing slurries may be selected to enhance the removal rate of a particular component on the surface of the wafer, taking into account that certain of the components may be inherently more easily removed purely by abrasive action.

While aluminum has been the preferred conductive metal used in semiconductor circuitry in the past, the more recent trend is towards the use of the damascene and dual damascene (also known as "inlaid metallization") process techniques that currently use copper, which is a superior electrical conductor. This trend towards using damascene and dual-damascene inlaying of metal lines and vias has presented new challenges in semiconductor

fabrication. It has been found that during CMP there is often unacceptable levels of "dishing" and erosion of copper surfaces. Indeed, depressions of about 1,000 Å or more may be formed.

As pointed out above, as near perfect a planar surface is needed to enable modern fine line circuits. Dishing and erosion therefore present a serious issue in the new damascene and dual damascene technology and a solution must be found.

Summary of The Invention

The invention presents a chemical-mechanical planarization technique that includes a first polishing step, and a second polishing step for use with wafers that include circuits formed by damascene and dual damascene processes. The second polishing step is especially important, and includes using a slurry that has a higher removal rate for dielectric than for metal.

More particularly, in accordance with the invention, in a first step the semiconductor wafer is polished with a polishing pad and a first slurry until an end point is detected. This end point may be detected by any of a variety of techniques known in the art, which may simply be the elapse of a predetermined polishing time period. Preferably, the detection is of a type that facilitates an automatic transition to the next stage in the CMP.

Preferably, after the first polishing step, the surface of the semiconductor wafer is rinsed to remove surface debris and substantially all of the first slurry. After rinsing, polishing recommences, with a second slurry that removes the dielectric at a higher rate than the metal component. It is preferred that the rate of dieletric removal should be from about 1.2 to about 4 times greater than the rate of metal removal.

It has been found that the second polishing step reduces dishing and erosion, and repairs nonuniformities in the initial wafer surface topography left after the first polishing step. As a consequence, dishing is substantially reduced and planarization of the semiconductor wafer surface is improved, thereby facilitating the production of a higher proportion of semiconductors that meet specifications.

Brief Description of The Drawings

Figure 1 is a schematic cross section of a surface portion of a semiconductor wafer formed by the damascene process showing trench structure in the dielectric onto which is formed a thin conformal barrier layer, onto which in turn is formed a layer of metal;

Figure 2 is a schematic illustration of the semiconductor wafer portion of Figure 1, after CMP has removed most of the metal layer;

Figure 3 is a schematic illustration of the semiconductor wafer portion of Figure 1 after

a CMP step has removed metal and was continued until excess metal was completely removed and recessed metal plugs were formed in the dielectric trenches;

Figure 4A is a schematic illustration of a cross sectional view of a portion of a semiconductor wafer as in Figure 1 after a first stage of CMP;

Figure 4B is a schematic illustration of the semiconductor wafer portion of Figure 4A after a second stage of CMP with a slurry having a selectivity ratio of 1:1:1 (metal:barrier:dielectric);

Figure 5A is a schematic illustration of a cross section of a portion of a semiconductor wafer as in Figure 1 after a first stage of CMP with a slurry, showing moderate dishing of the metal and metal residues on polished surfaces; and

Figure 5B is a schematic illustration of the semiconductor wafer section of Figure 5A after CMP with a second step slurry having a selectivity ratio of 1:1:2 (metal:barrier:dielectric) in accordance with the invention, showing repaired topography that is substantially planar.

Detailed Description of The Preferred Embodiments

The invention provides a chemical-mechanical planarization technique that substantially reduces "dishing" and "erosion" during the polishing of semiconductor wafers containing circuitry formed by the damascene and dual-damascene processes. The term "metal" as broadly used in the claims and specification refers to the conductive metal component of the wafer circuitry and may be formed from any of copper, silver, gold, and aluminum, each either in substantially pure form or as the major alloying component of an alloy, and also includes like conductive metals useful in the damascene and dual damascene processes. In accordance with the invention, two separate steps of chemical-mechanical polishing are used: A first step that removes substantially all excess metal that must be removed, and that is continued until a detected end point. This is followed by a second step of CMP that employs a slurry that has an about 1.2 to about 4 times higher removal rate for dielectric than the metal. Preferably, the dielectric removal rate is from about 1.5 to about 2.5 times higher than metal, and most preferably from about 1.8 to about 2.3 times higher than for metal. As explained in more detail below, the second step of polishing provides improved planarization, and substantially reduces the dishing and erosion found in prior art processes.

The invention may be better understood with reference to the attached drawings, some of which are illustrative of the invention, but which do not limit the scope of the invention as set forth in the specification and claims.

As a preliminary matter, Figure 1 illustrates a simplified schematic cross section through a portion of a semiconductor wafer surface produced by the damascene process,

showing three layers: An upper metal (for example, copper, aluminum, silver, gold, etc.) layer 2, formed on top of a conformal barrier (for example, tantalum) layer 4, on a dielectric (for example,an oxide such as TEOS) layer 6. This exemplary starting structure will be used to explain the invention, and contrast it with the one-step prior art CMP and an alternative two-step prior art CMP method.

Figure 2 shows the same wafer section after planarization using a 1-step slurry process. In this figure, there is a residual thin layer of metal 2 that extends above the barrier layer 4, that must yet be removed. Further polishing in the one-step process, utilizing a slurry that is selective for metal over dielectric, results in the structure shown in Figure 3. As can be seen, preferential metal removal has resulted in recessed metal plugs (i.e. dishing) formed in trenches in the dielectric.

As an alternative to the prior art one-step process described with reference to Figures 2 and 3, there is also a prior art two-step process, using in the first step a slurry with a greater removal rate for metal, for example a removal rate of metal about 20 times greater than for dielectric. An end point must first be selected for cessation for the first polishing step that is intended to remove the bulk of the metal shown in Figure 1 to achieve the structure show in Figure 4A. It is apparent that end point detection in polishing from the structure of Figure 1 to Figure 4A may not be possible, since the surface is still a substantially continuous layer of metal. Notwithstanding, based on experience, a polish time can be selected such that a thin metal layer is achieved. At that point, after rinsing to remove the first slurry, polishing could continue with a second slurry having a 1:1:1 selectivity to produce the structure shown in Figure 4B. The production of such a structure does, however, require a true 1:1:1 selectivity between the compositions in the semiconductor wafer surface undergoing polishing. These ratios must be stable with respect to both the process and the particular patterns on the wafer surface. Generally, the achievement of such stability is not common in practice.

The process in accordance with the invention is much more useful as a practical matter. According to the invention, after a first step of polishing that removes most of the excess metal shown in Figure 1, a structure such as that shown in Figure 5A is produced. This structure shows moderate dishing in that the metal 2 is recessed in trenches in the dielectric 6. Moreover, metal residues 8 may be left on the barrier surface. After rinsing, preferably with the deionized water, to substantially remove the first slurry from the polishing area, chemical-mechanical polishing continues with a second slurry in accordance with the invention, that has a higher selectivity (rate of removal) for dielectric relative to metal. Thus, for example, a second step slurry having a selectivity of 1:1:2 (with reference to metal:barrier:dielectric) produces the end

product shown in Figure 5B. In this figure, the metal residues 8 have been removed, the conformal horizontal barrier layer 4 has been removed, and the dielectric 6 has been polished level with the metal 2. Accordingly, the wafer surface is much more planar than that shown in the prior art of Figure 3.

The process of the invention is also much more convenient than the prior art process described with reference to Figures 4A and B in that it provides a readily detectible end point. Since the first step of polishing is carried out until substantially all excess metal is removed, optical, motor current monitoring or temperature monitoring techniques known in the art may be used to detect the end point. In contrast, since a thin layer of metal remains at the end of the first stage of the prior art method of Figure 4A, end point detection is difficult. Process time may be used to predict end point, but this depends upon maintaining substantial uniformity from one wafer to the next and is therefore not highly reliable.

As explained above, the process of the invention provides significant advantages over the prior art (Figure 3) and other possible two-step prior art techniques (Figures 4A and 4B) to provide improved planarization in a method that is readily automated.

Further, in accordance with the invention, existing CMP apparatus may be modified to use the two-step process of the invention. The required modifications would be readily apparent to those of skill in the art based on the above explanation of the invention.

The above explanation of the invention, with reference to the drawings, constitutes a description of preferred embodiments, and does not limit the scope of the invention which is determined by the entirety of this document and what its teachings would suggest to one of ordinary skill in the art, and by the appended claims, given their due scope.

In the claims:

1. A method of chemical-mechanical planarization of a surface of a semiconductor wafer containing metallic circuitry produced by a damascene or dual damascene process, the method comprising:

(i) polishing the wafer surface containing the metallic circuitry with a polishing pad and a first slurry;

(ii) detecting an end point for the polishing;

(iii) applying a rinse to the surface of the semiconductor wafer; and

(iv) polishing the surface of the semiconductor wafer with a second slurry having a greater selectivity for dielectric than for metal.

2. The method of claim 1, wherein the polishing of step (iv) comprises polishing with a second slurry having a removal rate of from about 1.2 to about 4 times greater for dielectric than for metal.

3. The method of claim 1, wherein the polishing of step (iv) comprises polishing with a second slurry having a removal rate of from about 1.5 to about 2.5 times greater for dielectric than for metal.

4. The method of claim 1, wherein the polishing of step (iv) comprises polishing with a second slurry having a removal rate of from about 1.8 to about 2.3 times greater for dielectric than for metal.

5. The method of claim 1, wherein the metallic circuitry comprises a metallic composition containing as its major component a metal selected from the group consisting of copper, silver, gold, and aluminum.

6. The method of claim 1, wherein the metallic circuitry comprises a metal selected from the group consisting of copper, silver, gold, and aluminum.

7. A method of chemical-mechanical polishing of a surface of a semiconductor wafer containing metallic circuitry formed by a damascene or dual damascene process, the method comprising:

(i) polishing the wafer surface with a polishing pad and a first slurry, the circuitry of the surface comprising a metal selected from the group consisting of copper, silver, gold, aluminum and alloys of these:

(ii) detecting an end point for polishing and preparing the wafer surface to receive a second slurry for a second step of polishing; and

(iii) polishing the wafer surface with a second slurry having a rate of removal of from

about 1.2 to about 4 times greater for dielectric than metal.

8. The method of claim 7, wherein the polishing with a second slurry comprises polishing with a slurry having a removal rate of from about 1.5 to about 2.5 times greater for dielectric than for metal.

9. The method of claim 7, wherein the polishing with a second slurry comprises polishing with a slurry having a removal rate of from about 1.8 to about 2.3 times greater for dielectric than for metal.

10. A method of chemical-mechanical planarization of a surface of a semiconductor wafer containing metallic circuitry produced by a damascene or dual damascene process, the method comprising:

(i) polishing the wafer surface containing the metallic circuitry with a polishing pad and a first slurry;

(ii) ceasing the polishing when a major portion of a metal layer on the surface of the wafer has been removed;

(iii) rinsing the polished surface of the wafer; and

(iv) polishing the rinsed surface of the wafer with a second slurry having a greater removal rate for dielectric than for metal.

11. The method of claim 10, wherein the polishing of step (iv) comprises polishing with a second slurry having a removal rate of about 1.2 to about 4 times greater for dielectric than for metal.

12. The method of claim 10, wherein the polishing of step (iv) comprises polishing with a slurry having a removal rate of about 1.5 to about 2.5 times greater for dielectric than metal.

13. The method of claim 10, wherein the polishing of step (iv) comprises polishing with a slurry having a removal rate of about 1.8 to about 2.3 times greater for dielectric than for metal.

14. The method of claim 10, wherein the metal circuitry comprises a metal selected from the group consisting of copper, gold, silver, aluminum and alloys of these.

1st-Step Slurry Planarization

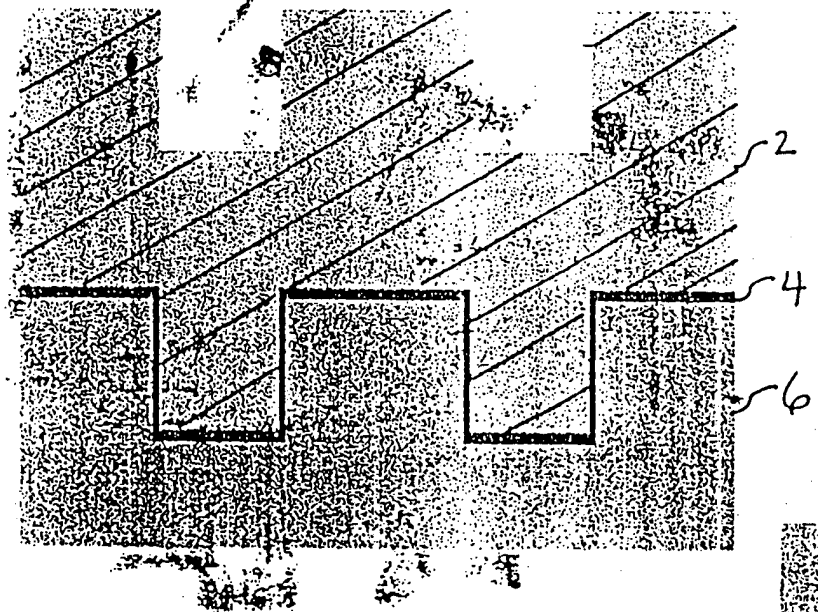

FIGURE 1

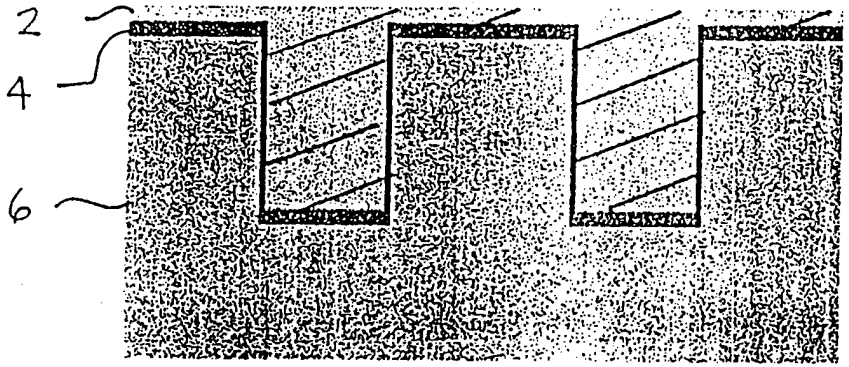

FIGURE 2

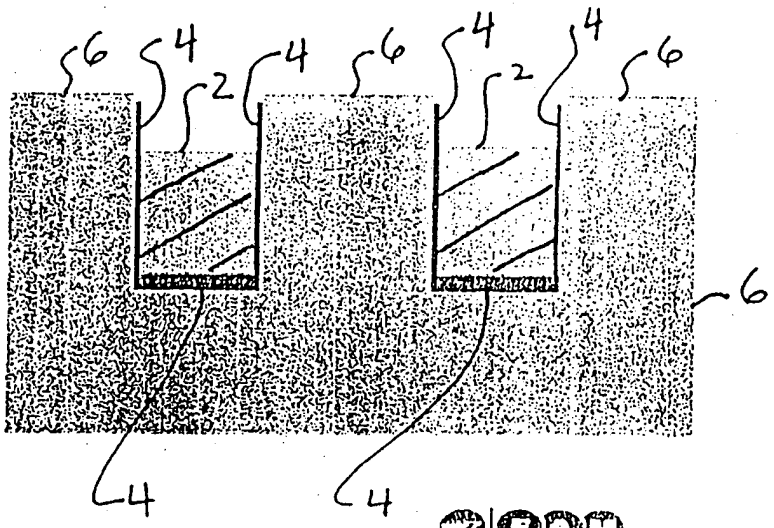

FIGURE 3

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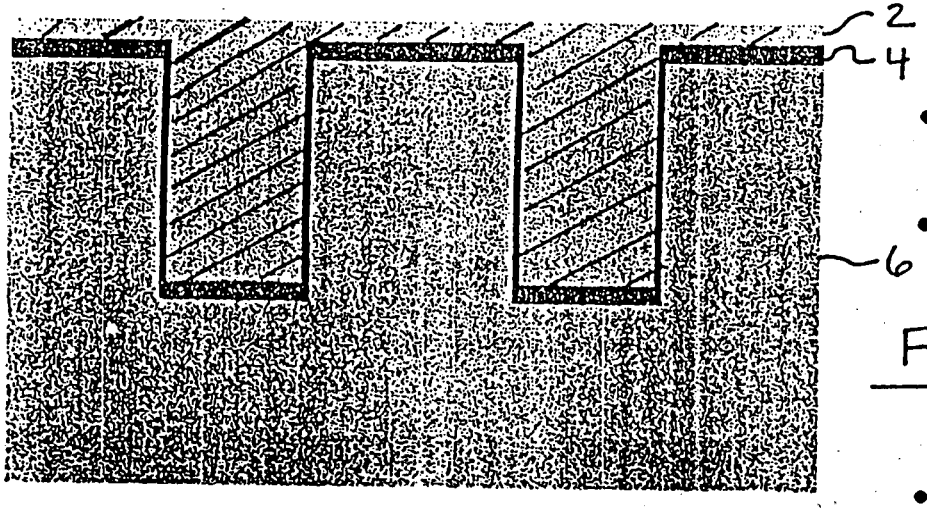
2nd-Step Slurry: 1:1:1 Selectivity



- Little EP capability
- Can use polish time

FIGURE 4A

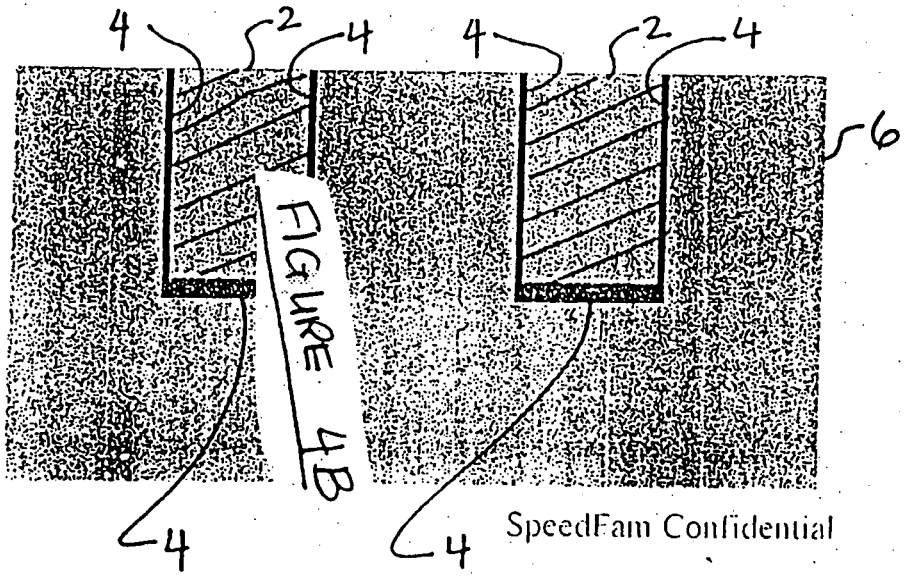


FIGURE 4B

- Requires true 1:1:1 selectivity
- Requires stable selectivity ratios wrt process and patterns

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2nd-Step Slurry: 1:1:2 Selectivity

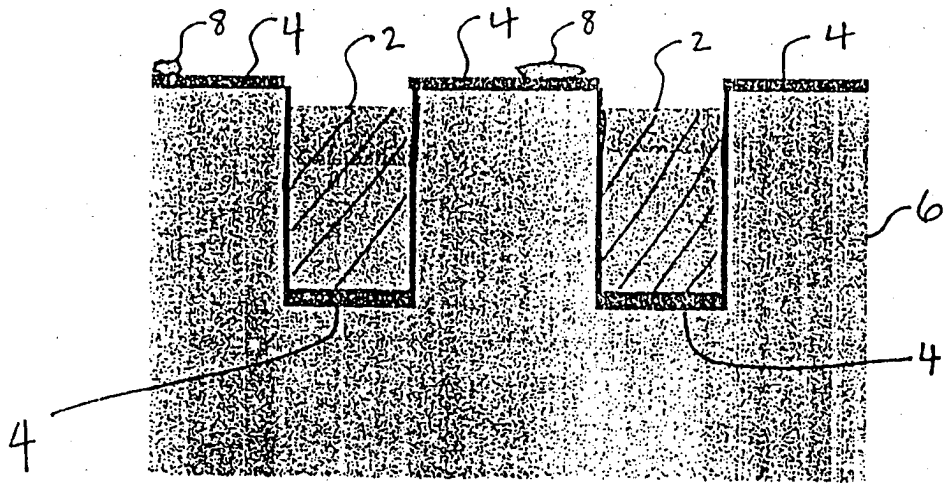

FIGURE 5A

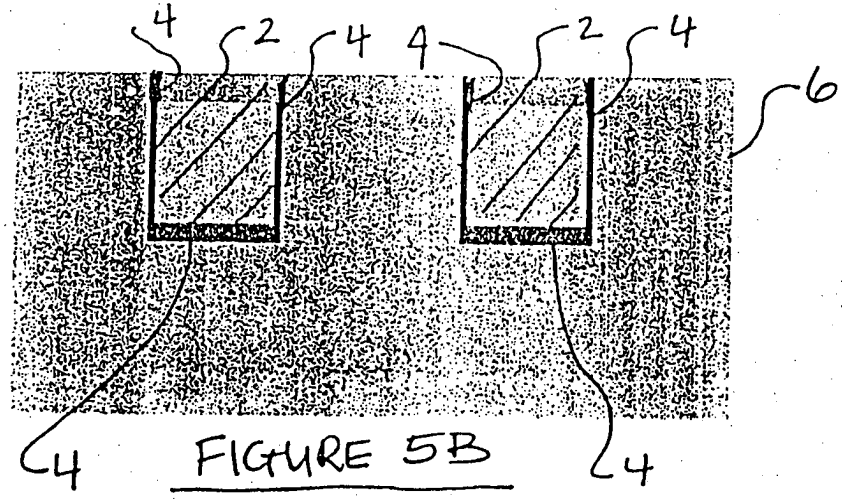

FIGURE 5B

- Moderate dishing
- Cu residues left
- Motor-current based EP capability

- Oxide polish rate > Cu rate 'repairs' initial topography

WO 00/59031

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PCT/US00/07652

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 00/07652

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

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Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

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